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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,969	09/07/2006	Mustafa Acar	NL04 0284 US1	4925

65913 7590 04/03/2008

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EXAMINER	
COLE, BRANDON S	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
04/03/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/591,969	ACAR ET AL.	
	Examiner	Art Unit	
	BRANDON S. COLE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *January 30th 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5 - 8 and 10 - 12* is/are rejected.

7)☒ Claim(s) *4 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *September 7th 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/7/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 1/30/08 has been received and entered in the case. In view of newly discovered prior art, new rejections are now set forth. Any inconvenience caused by the delay in citing this new prior art is regretted.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 -12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites a fifth and sixth transistor but doesn't provide antecedent basis for this because no first through fourth transistors have been set forth. Claims 9 -12 are rejected because they depend on claim 8.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 1, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US 6,166,571) in view of Koike (US 4,486,673).

As to claim 1, Wang figure 2 shows a frequency divider (master-slave flip flop) comprising a first latch (Q10,Q20, Q50, Q50', Q60, Q60', Q100) comprising a clock input (CLK') for receiving a clock signal, and a second latch (Q30,Q40, Q70, Q70', Q80, Q80', Q200), the second latch being crossed-coupled to the first latch, the second latch comprising a differential pair of transistors (A and A') for receiving a signal generated by the first latch.

Wang fails to show that the second latch is configured as a low-pass filter and that the second latch comprises a differential pair of transistors including a first pair of transistors comprising a first transistor coupled to second transistor a second pair of transistors comprising a third transistor coupled to a fourth transistor each transistor having a drain, a source and a gate, a drain of the first transistor and a drain of the third transistor being coupled to a source of the second transistor and to a source of the fourth transistor respectively gates of the second transistor and fourth transistor receiving a signal generated by the first

latch gates of the first transistor and the third transistor being coupled to a control signal for determining a low-pass characteristic of the second latch.

However, Koike figure 4 shows a latch comprising a differential pair of transistors including a first pair of transistors comprising a first transistor (Tr1) coupled to second transistor (Tr2) a second pair of transistors comprising a third transistor (Tr6) coupled to a fourth transistor (Tr7) each transistor having a drain, a source and a gate, a drain of the first transistor and a drain of the third transistor being coupled to a source of the second transistor and to a source of the fourth transistor respectively, gates of the second transistor and fourth transistor receiving a signal (fS and fR), and gates of the first transistor and the third transistor being coupled to a control signal (ØS and ØR). Koike teaches in column 1, lines 20 – 23 that figure 3 is a flip flop circuit.

It would have been obvious for someone having ordinary skill in the art at the time of the invention, to replace Wang's second latch with Koike's flip-flop for the purpose of enhancing its operation speed and reducing its current consumption.

The latch circuit being configured as a low-pass filter will be an inherent operational characteristic of the latches taught by Koike.

As to claim 5, Wang figure 2 shows a frequency divider wherein the control signal is a complementary clock signal (CLK') to the clock signal supplied to the first latch (Q10,Q20, Q50, Q50', Q60, Q60', Q100).

As to claim 6, Wang figure 2 shows a frequency divider wherein the first latch (Q10, Q20, Q50, Q50', Q60, Q60', Q100) is substantially identical to the second latch (Q30, Q40, Q70, Q70', Q80, Q80', Q200).

4. Claims 7, 8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (US 6,166,571) in view of (US 4,486,673) as applied to claim 1, and further in view of Yin et al (US 6,982,583).

As to claim 7, Wang figure 2 shows a frequency divider having first (Q10, Q20, Q50, Q50', Q60, Q60', Q100) and second latches (Q30, Q40, Q70, Q70', Q80, Q80', Q200).

Wang fails to show that each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor and between the drain of the fifth transistor and drain of the sixth transistor, respectively.

Yin et al shows that a first latch (802) comprises a negative resistance (RL1) coupled between the drains of said second transistor and fifth transistor and another negative resistance (RL2) coupled between the drain of the fourth transistor and drain of the sixth transistor, a second latch (804) comprising of a negative resistance (RL1A) coupled between the drains of said second transistor and fifth transistor and another negative resistance (RL2A) coupled between the drain of the fourth transistor and drain of the sixth transistor. Yin et al teaches in column 6, lines 60 – 67 that figure is a master-slave flip flop comprising of a first and second latch.

It would have been obvious for someone having ordinary skill in the art, at the time of the invention, to add a resistor between Wang's drains of the second transistor and fifth transistor and add another resistor between the drain of the fourth transistor and drain of the sixth transistor, on both latches for the purpose of enhancing the performance of the circuit.

As to claim 8, Wang figure 2 shows a frequency divider comprising, a first latch (Q10,Q20, Q50, Q50', Q60, Q60', Q100) comprising a clock input (CLK') for receiving a clock signal, and the second latch (Q30,Q40, Q70, Q70', Q80, Q80', Q200) being crossed-coupled to the first latch; wherein the second latch comprises a differential pair of transistors including a fifth transistor (Q70') and a sixth transistor (Q80') each transistor having a drain, a source and a gate, a drain of the fifth transistor and the drain of the sixth transistor being coupled to a supply voltage (Vdd), a source of the fifth transistor and a source of the sixth transistor being coupled to a common potential, that the drain of fifth transistor and the drain of the sixth transistor being coupled to a supply voltage, and the gates of the fifth transistor and sixth transistor receiving a signal generated (A and A') by the first latch.

Wang fails to show a second latch wherein the drain of fifth transistor and the drain of the sixth transistor being coupled to a supply voltage via respective resistors, and that the latch circuit configured as a low-pass filter,

However, Yin et al shows in figure 8 a first and a second latch wherein the drain of fifth transistor and the drain of the sixth transistor being coupled to a supply voltage via respective resistors (RL1A and RL2A). Yin et al teaches in

column 6, lines 60 – 67 that figure is a master-slave flip flop comprising of a first and second latch.

It would have been obvious for someone having ordinary skill in the art, at the time of the invention, to add a resistor between Wang's drains of the fifth transistor and sixth transistor of the second latch for the purpose of enhancing the performance of the circuit.

The latch circuit being configured as a low-pass filter will be an inherent operational characteristic of the latches taught by Yin et al.

As to claim 10, Wang figure 2 shows a frequency divider wherein the control signal is a complementary clock signal (CLK') to the clock signal supplied to the first latch (Q10,Q20, Q50, Q50', Q60, Q60', Q100).

As to claim 11, Wang figure 2 shows a frequency divider wherein the first latch (Q10, Q20, Q50, Q50', Q60, Q60', Q100) is substantially identical to the second latch (Q30, Q40, Q70, Q70', Q80, Q80', Q200).

As to claim 12, Wang figure 2 shows a frequency divider it a first (Q10, Q20, Q50, Q50', Q60, Q60', Q100) and second latch (Q30, Q40, Q70, Q70', Q80, Q80', Q200).

Wang fails to show that each latch comprises a negative resistance coupled between the drains of said second transistor and said fourth transistor and between the drain of the fifth transistor and drain of the sixth transistor, respectively.

Yin et al shows that a first latch (802) comprises a negative resistance (RL1) coupled between the drains of said second transistor and fifth transistor

and another negative resistance (RL2) coupled between the drain of the fourth transistor and drain of the sixth transistor, a second latch (804) comprising of a negative resistance (RL1A) coupled between the drains of said second transistor and fifth transistor and another negative resistance (RL2A) coupled between the drain of the fourth transistor and drain of the sixth transistor. Yin et al teaches in column 6, lines 60 – 67 that figure is a master-slave flip flop comprising of a first and second latch.

It would have been obvious for someone having ordinary skill in the art, at the time of the invention, to add a resistor between Wang' drains of the second transistor and fifth transistor and add another resistor between the drain of the fourth transistor and drain of the sixth transistor, on both latches for the purpose of enhancing the performance of the circuit.

Allowable Subject Matter

5. Claims 4 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is (571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards, can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth B. Wells/
Primary Examiner
Art Unit 2816

/Brandon S Cole/
Examiner, Art Unit 2816